**UVM Verification Plan**

**1. SPI Interface Overview**

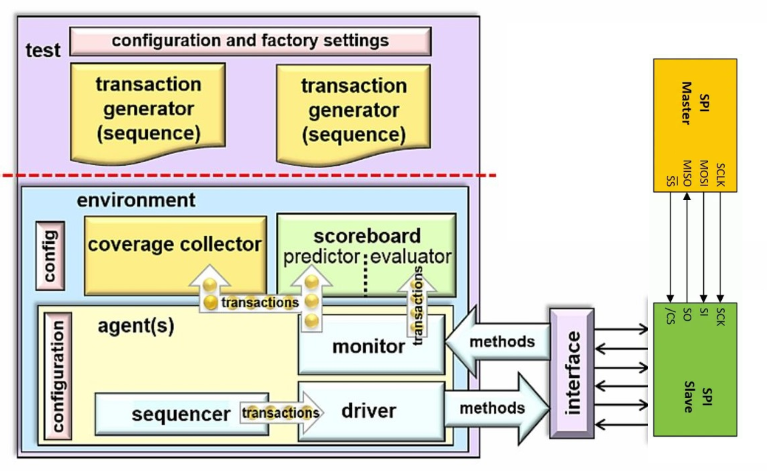
SPI is a full-duplex, synchronous serial communication protocol with the following key signals:

| **Signal** | **Direction** | **Description** |
| --- | --- | --- |
| mclk (CLK) | Master → Slave | Serial clock (generated by master) |
| mosi (Master Out Slave In) | Master → Slave | Data from master to slave |
| miso (Master In Slave Out) | Slave → Master | Data from slave to master |
| cs (Chip Select) | Master → Slave | Active-low slave select signal |
| reset | Global | Active-low asynchronous reset |

**2. Test Case Overview**

| **Test Case** | **Description** | **Key Verification Points** |
| --- | --- | --- |
| Full Duplex | Simultaneous master-to-slave and slave-to-master transfer | Bidirectional data integrity, protocol timing |
| Only Master Load | Master transmits data while slave only receives (no slave load) | Master transmission correctness |
| Only Slave Load | Slave transmits data while master only receives (no master load) | Slave transmission correctness |
| No Load | Neither master nor slave loads new data (verify idle behavior) | Signal stability in idle state |
| Master Active | Slave remains idle | Simulate slave device error or disconnection |
| Slave Active | Master remains idle | Simulate master error (overall SPI error) |

**3. Block Diagram**

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